12.2.4 MODBUS Register Mapping

The following tables display the MODBUS addressing and the corresponding IEC61131 addressing for the process image, the PFC variables, the NOVRAM data, and the internal variables is represented.

Via the register services the states of the complex and digital I/O modules can be determined or changed.

Register Access Reading (with FC3, FC4 and FC23)

Table 117: Register access reading (with FC3, FC4 and FC23)

MODBUS address		IEC 61131	Memory range
[dec]	[hex]	address	
0...255	0x0000...0x00FF	%IW0...%IW255	Physical input area (1) First 256 words of physical input data
256...511	0x0100...0x01FF	%QW256...%QW511	PFC OUT area Volatile PFC output variables
512...767	0x0200...0x02FF	%QW0...%QW255	Physical output area (1) First 256 words of physical output data
768...1023	0x0300...0x03FF	%IW256...%IW511	PFC IN area Volatile PFC input variables
1024...4095	0x0400...0x0FFF	-	MODBUS exception: “Illegal data address”
4096...12287	0x1000...0x2FFF	-	Configuration register (see following chapter “Configuration Functions“)
12288...24575	0x3000...0x5FFF	%MW0...%MW12287	NOVRAM 24 kB retain memory *) *) In Target settings RETAIN on 0, flags on MAX (24 kB)
24576...25340	0x6000...0x62FC	%IW512...%IW1275	Physical input area (2) Additional 764 words physical input data
25341...28671	0x62FD...0x6FFF	-	MODBUS exception: “Illegal data address”
28672...29436	0x7000...0x72FC	%QW512...%QW1275	Physical output area (2) Additional 764 words physical output data
29437...65535	0x72FD...0xFFFF	-	MODBUS exception: “Illegal data address”

Register Access Writing (with FC6, FC16, FC22 and FC23)

Table 118: Register access writing (with FC6, FC16, FC22 and FC23)

MODBUS address		IEC 61131	Memory range
[dec]	[hex]	address	
0...255	0x0000...0x00FF	%QW0...%QW255	Physical output area (1) First 256 words of physical output data
256...511	0x0100...0x01FF	%IW256...%IW511	PFC IN area Volatile PFC input variables
512...767	0x0200...0x02FF	%QW0...%QW255	Physical output area (1) First 256 words of physical output data
768...1023	0x0300...0x03FF	%IW256...%IW511	PFC IN area Volatile PFC input variables
1024...4095	0x0400...0x0FFF	-	MODBUS exception: “Illegal data address”
4096...12287	0x1000...0x2FFF	-	Configuration register (see following chapter „Configuration Functions“)
12288...24575	0x3000...0x5FFF	%MW0...%MW12287	NOVRAM 24 kB retain memory *) *) In Target settings RETAIN on 0, flags on MAX (24 kB)
24576...25340	0x6000...0x62FC	%QW512...%QW1275	Physical output area (2) Additional 764 words physical output data
25341...28671	0x62FD...0x6FFF	-	MODBUS exception: “Illegal data address”
28672...29436	0x7000...0x72FC	%QW512...%QW1275	Physical output area (2) Additional 764 words physical output data
29437...65535	0x72FD...0xFFFF	-	MODBUS exception: “Illegal data address”

The digital MODBUS services (coil services) are bit accesses, with which only the states of digital I/O modules can be determined or changed. Complex I/O modules are not attainable with these services and so they are ignored. Because of this the addressing of the digital channels begins again with 0, so that the MODBUS address is always identical to the channel number, (i.e. the digital input no. 47 has the MODBUS address "46").

Bit Access Reading (with FC1 and FC2)

Table 119: Bit access reading (with FC1 and FC2)

MODBUS address [dec]	MODBUS address [hex]	Memory range	Description
0...511	0x0000...0x01FF	Physical input area (1)	First 512 digital inputs
512...1023	0x0200...0x03FF	Physical output area (1)	First 512 digital outputs
1024...4095	0x0400...0x0FFF	-	MODBUS exception: “Illegal data address”
4096...8191	0x1000...0x1FFF	%QX256.0...%QX511.15	PFC OUT area Volatile PFC output variables
8192...12287	0x2000...0x2FFF	%IX256.0...%IX511.15	PFC IN area Volatile PFC input variables
12288...32767	0x3000...0x7FFF	%MX0...%MX1279.15	NOVRAM 2 kB retain memory (max. 24 kB)
32768...34295	0x8000...0x85F7	Physical input area (2)	Starts with the 513th and ends with the 2039th digital input
34296...36863	0x85F8...0x8FFF	-	MODBUS exception: “Illegal data address”
36864...38391	0x9000...0x95F7	Physical output area (2)	Starts with the 513th and ends with the 2039th digital output
38392...65535	0x95F8...0xFFFF	-	MODBUS exception: “Illegal data address”

Bit Access Writing (with FC5 and FC15)

Table 120: Bit access writing (with FC5 and FC15)

MODBUS address [dez]	MODBUS address [hex]	Memory Range	Description
0...511	0x0000...0x01FF	Physical output area (1)	First 512 digital outputs
512...1023	0x0200...0x03FF	Physical output area (1)	First 512 digital outputs
1024...4095	0x0400...0x0FFF	-	MODBUS exception: “Illegal data address”
4096...8191	0x1000...0x1FFF	%IX256.0...%IX511.15	PFC IN area Volatile PFC input variables
8192...12287	0x2000...0x2FFF	%IX256.0...%IX511.15	PFC IN area Volatile PFC input variables
12288...32767	0x3000...0x7FFF	%MX0...%MX1279.15	NOVRAM 2 kB retain memory
32768...34295	0x8000...0x85F7	Physical output area (2)	Starts with the 513th and ends with the 2039 th digital input
34296...36863	0x85F8...0x8FFF	-	MODBUS-Exception: “Illegal data address”
36864...38391	0x9000...0x95F7	Physical output area (2)	Starts with the 513 th and ends with the 2039 th digital output
38392...65535	0x95F8...0xFFFF	-	MODBUS-Exception: “Illegal data address”

12.2.5 MODBUS Registers

Table 121: MODBUS registers

Register address	Access	Length (Word)	Description
0x1000	R/W	1	Watchdog time read/write
0x1001	R/W	1	Watchdog coding mask 1…16
0x1002	R/W	1	Watchdog coding mask 17…32
0x1003	R/W	1	Watchdog trigger
0x1004	R	1	Minimum trigger time
0x1005	R/W	1	Watchdog stop (Write sequence 0xAAAA, 0x5555)
0x1006	R	1	Watchdog status
0x1007	R/W	1	Restart watchdog (Write sequence 0x1)
0x1008	R/W	1	Stop watchdog (Write sequence 0x55AA or 0xAA55)
0x1009	R/W	1	MODBUS and HTTP close at watchdog time-out
0x100A	R/W	1	Watchdog configuration
0x100B	W	1	Save watchdog parameter
0x1020	R	1…2	LED error code
0x1021	R	1	LED error argument
0x1022	R	1…4	Number of analog output data in the process image (in bits)
0x1023	R	1…3	Number of analog input data in the process image (in bits)
0x1024	R	1…2	Number of digital output data in the process image (in bits)
0x1025	R	1…4	Number of digital input data in the process image (in bits)
0x1028	R/W	1	Boot configuration
0x1029	R	9	MODBUS/TCP statistics
0x102A	R	1	Number of TCP connections
0x102B	W	1	KBUS Reset
0x1030	R/W	1	Configuration MODBUS/TCP time-out
0x1031	R	3	Read out the MAC-ID of the coupler/controller
0x1035	R/W	1	Timeoffset RTC
0x1036	R/W	1	Daylight Saving
0x1037	R/W	1	Modbus Response Delay (ms)
0x1050	R	3	Diagnosis of the connected I/O modules
0x2000	R	1	Constant 0x0000
0x2001	R	1	Constant 0xFFFF
0x2002	R	1	Constant 0x1234
0x2003	R	1	Constant 0xAAAA
0x2004	R	1	Constant 0x5555
0x2005	R	1	Constant 0x7FFF
0x2006	R	1	Constant 0x8000
0x2007	R	1	Constant 0x3FFF
0x2008	R	1	Constant 0x4000
0x2010	R	1	Firmware version
0x2011	R	1	Series code
0x2012	R	1	Coupler/controller code
0x2013	R	1	Firmware version major revision
0x2014	R	1	Firmware version minor revision

Table 122: MODBUS registers (Continuation)

Register address	Access	Length (Word)	Description
0x2020	R	16	Short description controller
0x2021	R	8	Compile time of the firmware
0x2022	R	8	Compile date of the firmware
0x2023	R	32	Indication of the firmware loader
0x2030	R	65	Description of the connected I/O modules (module 0…64)
0x2031	R	64	Description of the connected I/O modules (module 65…128)
0x2032	R	64	Description of the connected I/O modules (module 129…192)
0x2033	R	63	Description of the connected I/O modules (module 193…255)
0x2040	W	1	Software reset (Write sequence 0x55AA or 0xAA55)
0x2041	W	1	Format flash disk
0x2042	W	1	Extract HTML sides from the firmware
0x2043	W	1	Factory settings

12.2.5.1 Accessing Register Values

You can use any MODBUS application to access (read from or write to) register values. Both commercial (e.g., "Modscan") and free programs (from http://www.modbus.org/tech.php) are available.

The following sections describe how to access both the registers and their values.

12.2.5.2 Watchdog Registers

The watchdog monitors the data transfer between the fieldbus master and the controller. Every time the controller receives a specific request (as define in the watchdog setup registers) from the master, the watchdog timer in the controller resets.

In the case of fault free communication, the watchdog timer does not reach its end value. After each successful data transfer, the timer is reset.

If the watchdog times out, a fieldbus failure has occurred. In this case, the fieldbus controller answers all following MODBUS TCP/IP requests with the exception code 0x0004 (Slave Device Failure).

In the controller special registers are used to setup the watchdog by the master (Register addresses 0x1000 to 0x1008).

By default, the watchdog is not enabled when you turn the controller on. To activate it, the first step is to set/verify the desired time-out value of the Watchdog Time register (0x1000). Second, the function code mask must be specified in the mask register (0x1001), which defines the function code(s) that will reset the timer. Finally, the Watchdog-Trigger register (0x1003) must be changed to a non-zero value to start the timer.

Reading the Minimum Trigger time (Register 0x1004) reveals whether a watchdog fault occurred. If this time value is 0, a fieldbus failure is assumed. The timer of watchdog can manually be reset, if it is not timed out, by writing a value of 0x1 to the Restart Watchdog register (0x1007).

After the watchdog is started, it can be stopped by the user via the Watchdog Stop register (0x1005) or the Simply Stop Watchdog register (0x1008).

The watchdog registers can be addressed in the same way as described with the MODBUS read and write function codes. Specify the respective register address in place of the reference number.

Table 123: Register address 0x1000

Register address 0x1000 (4096_{dec})	
Value	Watchdog time, WS_TIME
Access	Read/write
Default	0x0064
Description	This register stores the watchdog timeout value as an unsigned 16 bit value. The default value is 0. Setting this value will not trigger the watchdog. However, a non zero value must be stored in this register before the watchdog can be triggered. The time value is stored in multiples of 100ms (e.g., 0x0009 is .9 seconds). It is not possible to modify this value while the watchdog is running.

Table 124: Register address 0x1001

Register address 0x1001 (4097_{dec})	
Value	Watchdog function coding mask, function code 1...16, WDFCM_1_16
Access	Read/write
Default	0xFFFF
Description	Using this mask, the function codes can be set to trigger the watchdog function. The function code can be selected via a "1" FC 1 Bit 0 FC 2 Bit 1 FC 3 Bit 0 or 1 FC 4 Bit 2 FC 5 Bit 0 or 2 FC 6 Bit 1 or 2 etc. The watchdog function is started if a value is not equal to zero. If only codes from non-supported functions are entered in the mask, the watchdog will not start. An existing fault is reset and writing into the process illustration is possible. Also here changes cannot be made while the watchdog is running. When the watchdog is enabled, no code is generated to rewrite the current data value.

Table 125: Register address 0x1002

Register address 0x1002 (4098_{dec})	
Value	Watchdog function coding mask, function code 17...32, WD_FCM_17_32
Access	Read/write
Default	0xFFFF
Description	Same function as above, however, with the function codes 17 to 32. These codes are currently not supported, for this reason the default value should not be changed. It is not possible to modify this value while the watchdog is running.

Table 126: Register address 0x1003

Register address 0x1003 (4099_{dez})	
Value	Watchdog Trigger, WD_TRIGGER
Access	Read/write
Standard	0x0000
Description	This register is used for an alternative trigger method. The watchdog is triggered by writing different values in this register. Values following each other must differ in size. Writing of a value not equal to zero starts the watchdog. A watchdog fault is reset and writing process data is possible again.

Table 127: Register address 0x1004

Register address 0x1004 (4100_{dez})	
Value	Minimum current trigger time, WD_AC_TRG_TIME
Access	Read/write
Standard	0xFFFF
Description	This register saves the minimum current watchdog trigger time. If the watchdog is triggered, the saved value is compared with the current value. If the current value is smaller than the saved value, this is replaced by the current value. The unit is 100 ms/digit. The saved value is changed by writing new values, which does not affect the watchdog. 0x000 is not permissible.

Table 128: Register address 0x1005

Register address 0x1005 (4101_{dez})	
Value	Stop watchdog, WD_AC_STOP_MASK
Access	Read/write
Standard	0x0000
Description	The watchdog is stopped if here the value 0xAAAA is written first, followed by 0x5555. The watchdog fault reaction is blocked. A watchdog fault is reset and writing on the process data is possible again.

Table 129: Register address 0x1006

Register address 0x1006 (4102_{dez})	
Value	While watchdog is running, WD_RUNNING
Access	Read
Standard	0x0000
Description	Current watchdog status. at 0x0000: Watchdog not active at 0x0001: Watchdog active at 0x0002: Watchdog exhausted.

Table 130: Register address 0x1007

Register address 0x1007 (4103_{dez})	
Value	Restart watchdog, WD_RESTART
Access	Read/write
Standard	0x0001
Description	This register restarts the watchdog timer by writing a value of 0x1 into it. If the watchdog was stopped before the overrun, it is not restarted.

Table 131: Register address 0x1008

Register address 0x1008 (4104_{dez})	
Value	Simply stop watchdog, WD_AC_STOP_SIMPLE
Access	Read/write
Standard	0x0000
Description	This register stops the watchdog by writing the value 0x0AA55 or 0X55AA into it. The watchdog timeout fault is deactivated and it is possible to write in the watchdog register again. If there is an existing watchdog fault, it is reset

Table 132: Register address 0x1009

Register address 0x1009 (4105_{dez})	
Value	Close MODBUS socket after watchdog timeout
Access	Read/write
Description	0: MODBUS socket is not closed 1: MODBUS socket is closed

Table 133: Register address 0x100A

Register address 0x100A (4106_{dez})	
Value	Alternative watchdog
Access	Read/write
Standard	0x0000
Description	This register provides an alternate way to activate the watchdog timer. Procedure: Write a time value in register 0x1000; then write a 0x0001 into register 0x100A. With the first MODBUS request, the watchdog is started. The watchdog timer is reset with each MODBUS/TCP instruction. If the watchdog times out, all outputs are set to zero. The outputs will become operational again, after communications are re-established. Register 0x00A is non-volatile, including register 0x1000. It is not possible to modify the time value in register 0x1000 while the watchdog is running.

The length of each register is 1 word; i.e., with each access only one word can be written or read. Following are two examples of how to set the value for a time overrun:

Setting the watchdog for a timeout of more than 1 second:

1. Write 0x000A in the register for time overrun (0x1000).
   Register 0x1000 works with a multiple of 100 ms;
   1 s = 1000 ms; 1000 ms / 100 ms = 10_{dec} = A_{hex})

2. Use the function code 5 to write 0x0010 (=2(5-1)) in the coding mask (register 0x1001).

Table 134: Starting Watchdog

FC	FC16	FC15	FC14	FC13	FC12	FC11	FC10	FC9	FC8	FC7	FC6	**FC5**	FC4	FC3	FC2	FC1
Bit	15	14	13	12	11	10	9	8	7	6	5	**4**	3	2	1	0
bin	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0
hex	0				0				**1**				0			

Function code 5 (writing a digital output bit) continuously triggers the watchdog to restart the watchdog timer again and again within the specified time. If time between requests exceeds 1 second, a watchdog timeout error occurs.

3. To stop the watchdog, write the value 0x0AA55 or 0X55AA into 0x1008 (Simply Stop Watchdog register, WD_AC_STOP_SIMPLE).

Setting the watchdog for a timeout of 10 minutes or more:

1. Write 0x1770 (= 10*60*1000 ms / 100 ms) in the register for time overrun (0x1000).
   (Register 0x1000 works with a multiple of 100 ms;
   10 min = 600,000 ms; 600,000 ms / 100 ms = 6000dec = 1770hex)

2. Write 0x0001 in the watchdog trigger register (0x1003) to start the watchdog.

3. Write different values (e.g., counter values 0x0000, 0x0001) in the watchdog to trigger register (0x1003).

Values following each other must differ in size. Writing of a value not equal to zero starts the watchdog. Watchdog faults are reset and writing process data is possible again.

4. To stop the watchdog, write the value 0x0AA55 or 0X55AA into 0x1008 (Simply Stop Watchdog register, WD_AC_STOP_SIMPLE).

Table 135: Register address 0x100B

Register address 0x100B (4107_{dez})	
Value	Save watchdog parameter
Access	Write
Standard	0x0000
Description	With writing of '0x55AA' or '0xAA55' in register 0x100B the registers 0x1000, 0x1001, 0x1002 are set on remanent.

12.2.5.3 Diagnostic Registers

The following registers can be read to determine errors in the node:

Table 136: Register address 0x1020

Register address 0x1020 (4128_{dec})	
Value	LedErrCode
Access	Read
Description	Declaration of the Error code

Table 137: Register address 0x1021

Register address 0x1021 (4129_{dec})	
Value	LedErrArg
Access	Read
Description	Declaration of the Error argument

12.2.5.4 Configuration Registers

The following registers contain configuration information of the connected modules:

Table 138: Register address 0x1022

Register address 0x1022 (4130_{dec})	
Value	CnfLen.AnalogOut
Access	Read
Description	Number of word-based outputs registers in the process image in bits (divide by 16 to get the total number of analog words)

Table 139: Register address 0x1023

Register address 0x1023 (4131_{dec})	
Value	CnfLen.AnalogInp
Access	Read
Description	Number of word-based inputs registers in the process image in bits (divide by 16 to get the total number of analog words)

Table 140: Register address 0x1024

Register address 0x1024 (4132_{dec})	
Value	CnfLen.DigitalOut
Access	Read
Description	Number of digital output bits in the process image

Table 141: Register address 0x1025

Register address 0x1025 (4133_{dec})	
Value	CnfLen.DigitalInp
Access	Read
Description	Number of digital input bits in the process image

Table 142: Register address 0x1028

Register address 0x1028 (4136_{dec})	
Value	Boot options
Access	Read/write
Description	Boot configuration: 1: BootP 2: DHCP 4: EEPROM

Table 143: Register address 0x1029

Register address 0x1029 (4137_{dec}) with 9 words	
Value	MODBUS TCP statistics
Access	Read/write
Description	1 word SlaveDeviceFailure → internal bus error, fieldbus error by activated watchdog 1 word BadProtocol → error in the MODBUS TCP header 1 word BadLength → Wrong telegram length 1 word BadFunction → Invalid function code 1 word BadAddress → Invalid register address 1 word BadData → Invalid value 1 word TooManyRegisters → Number of the registers which can be worked on is too large, Read/Write 125/100 1 word TooManyBits → Number of the coils which can be worked on is too large, Read/Write 2000/800 1 word ModTcpMessageCounter → Number of received MODBUS/TCP requests With Writing 0xAA55 or 0x55AA in the register will reset this data area.

Table 144: Register address 0x102A

Register address 0x102A (4138_{dec}) with a word count of 1	
Value	MODBUS/TCP Connections
Access	Read
Description	Number of TCP connections

Table 145: Register address 0x102B

Register address 0x102B (4139_{dez}) with a word count of up to 1	
Value	KBUS reset
Access	Write
Description	Writing of this register restarts the internal bus

Table 146: Register address 0x1030

Register address 0x1030 (4144_{dec}) with a word count of 1	
Value	Configuration MODBUS/TCP Time-out
Access	Read/write
Default	0x0258 (600 decimal)
Description	This is the maximum number of milliseconds the fieldbus coupler will allow a MODBUS/TCP connection to stay open without receiving a MODBUS request. Upon time-out, idle connection will be closed. Outputs remain in last state. Default value is 600 ms (60 seconds), the time base is 100 ms, the minimal value is 100 ms. If the value is set to ‘0’, the timeout is disabled. On this connection, the watchdog is triggered with a request.

Table 147: Register address 0x1031

Register address 0x1031 (4145_{dec}) with a word count of 3	
Value	Read the MAC-ID of the controller
Access	Read
Description	This register gives the MAC-ID, with a length of 3 words

Table 1: Register address 0x1035

Register address 0x1035 (4149_{dez}) 1 Word	
Value	Configuration of the time offsets to the GMT time
Access	Read/write
Default	0x0000
Description	Register to set the time offset to the UTC time (Greenwich meridian) with a possible setting range from -12 to +12.

Table 1: Register address 0x1036

Register address 0x1036 (4150_{dez}) 1 Word	
Value	Configuration of summer or winter time
Access	Read/write
Default	0x0000
Description	Register to set winter or summer time (Daylight Saving Time). The values 0 and 1 are valid.

Table 1: Register address 0x1037

Register address 0x1031 (4151_{dez}) with a word count of 3	
Value	Configuration of Modbus Response Delay Time
Access	Read/write
Default	0x0000
Description	This register saves the value for the Modbus Response Delay Time for a Modbus connection. The time base is 1 ms. On the Modbus TCP connection, the response will be delayed by the inscribed time.

Table 148: Register address 0x1050

Register address 0x1050 (4176_{dec}) with a word count of 3 **since Firmware version 9**	
Value	Diagnosis of the connected I/O modules
Access	Read
Description	Diagnosis of the connected I/O modules, length 3 words Word 1: Number of the module Word 2: Number of the channel Word 3: Diagnosis

Table 149: Register address 0x2030

Register address 0x2030 (8240_{dec}) with a word count of up to 65																
Value	Description of the connected I/O modules															
Access	Read module 0...64															
Description	Length 1...65 words These 65 registers identify the controller and the first 64 modules present in a node. Each module is represented in a word. Because item numbers cannot be read out of digital modules, a code is displayed for them, as defined below: Bit position 0 → Input module Bit position 1 → Output module Bit position 2…7 → Not used Bit position 8…14 → Module size in bits Bit position 15 → Designation digital module															
	Examples:															
	4 Channel Digital Input Module = 0x8401															
	Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Code	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1
	Hex	8				4				0				1			
	2 Channel Digital Output Module = 0x8202																
	Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Code	1	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0
	Hex	8				2				0				2			

Table 150: Register address 0x2031

Register address 0x2031 (8241_{dec}) with a word count of up to 64	
Value	Description of the connected I/O modules
Access	Read modules 65...128
Description	Length 1-64 words These 64 registers identify the 2nd block of I/O modules present (modules 65 to 128). Each module is represented in a word. Because item numbers cannot be read out of digital modules, a code is displayed for them, as defined below: Bit position 0 → Input module Bit position 1 → Output module Bit position 2…7 → Not used Bit position 8…14 → Module size in bits Bit position 15 → Designation digital module

Table 151: Register address 0x2032

Register address 0x2032 (8242_{dec}) with a word count of up to 64	
Value	Description of the connected I/O modules
Access	Read modules 129...192
Description	Length 1…64 words These 64 registers identify the 3rd block of I/O modules present (modules 129 to 192). Each module is represented in a word. Because item numbers cannot be read out of digital modules, a code is displayed for them, as defined below: Bit position 0 → Input module Bit position 1 → Output module Bit position 2…7 → Not used Bit position 8…14 → Module size in bits Bit position 15 → Designation digital module

Table 152: Register address 0x2033

Register address 0x2033 (8243_{dec}) with a word count of up to 65	
Value	Description of the connected I/O modules
Access	Read modules 193 ... 255
Description	Length 1-63 words These 63 registers identify the 4th block of I/O modules present (modules 193 to 255). Each module is represented in a word. Because item numbers cannot be read out of digital modules, a code is displayed for them, as defined below: Bit position 0 → Input module Bit position 1 → Output module Bit position 2…7 → Not used Bit position 8…14 → Module size in bits Bit position 15 → Designation digital module

Table 153: Register address 0x2040

Register address 0x2040 (8256_{dec})	
Value	Implement a software reset
Access	Write (Write sequence 0xAA55 or 0x55AA)
Description	With Writing 0xAA55 or 0x55AA the register will be reset.

Table 154: Register address 0x2041

Register address 0x2041 (8257_{dez})	
Value	Flash Format
Access	Write (Write sequence 0xAA55 or 0x55AA)
Description	The file system Flash is again formatted.

Table 155: Register address 0x2042

Register address 0x2042 (8258_{dez})	
Value	Extract data files
Access	Write (Write sequence 0xAA55 or 0x55AA)
Description	The standard files (HTML pages) of the Coupler/Controller are extracted and written into the Flash.

Table 156: Register address 0x2043

Register address 0x2043 (8259_{dez})	
Value	0x55AA
Access	Write
Description	Factory Settings

12.2.5.5 Firmware Information Registers

The following registers contain information on the firmware of the controller:

Table 157: Register address 0x2010

Register address 0x2010 (8208_{dec}) with a word count of 1	
Value	Revision, INFO_REVISION
Access	Read
Description	Firmware index, e.g. 0005 for version 5

Table 158: Register address 0x2011

Register address 0x2011 (8209_{dec}) with a word count of 1	
Value	Series code, INFO_SERIES
Access	Read
Description	WAGO serial number, e.g. 0750 for WAGO-I/O-SYSTEM 750

Table 159: Register address 0x2012

Register address 0x2012 (8210_{dec}) with a word count of 1	
Value	Item number, INFO_ITEM
Access	Read
Description	WAGO item number, e.g. 841 for the controller 750-841 or 341 for the coupler 750-341 etc.

Table 160: Register address 0x2013

Register address 0x2013 (8211_{dec}) with a word count of 1	
Value	Major sub item code, INFO_MAJOR
Access	Read
Description	Firmware version Major Revision

Table 161: Register address 0x2014

Register address 0x2014 (8212_{dec}) with a word count of 1	
Value	Minor sub item code, INFO_MINOR
Access	Read
Description	Firmware version Minor Revision

Table 162: Register address 0x2020

Register address 0x2020 (8224_{dec}) with a word count of up to 16	
Value	Description, INFO_DESCRIPTION
Access	Read
Description	Information on the controller, 16 words

Table 163: Register address 0x2021

Register address 0x2021 (8225_{dec}) with a word count of up to 8	
Value	Description, INFO_DESCRIPTION
Access	Read
Description	Time of the firmware version, 8 words

Table 164: Register address 0x2022

Register address 0x2022 (8226_{dec}) with a word count of up to 8	
Value	Description, INFO_DATE
Access	Read
Description	Date of the firmware version, 8 words

Table 165: Register address 0x2023

Register address 0x2023 (8227_{dec}) with a word count of up to 32	
Value	Description, INFO_LOADER_INFO
Access	Read
Description	Information to the programming of the firmware, 32 words

12.2.5.6 Constant Registers

The following registers contain constants, which can be used to test communication with the master:

Table 166: Register address 0x2000

Register address 0x2000 (8192_{dec})	
Value	Zero, GP_ZERO
Access	Read
Description	Constant with zeros

Table 167: Register address 0x2001

Register address 0x2001 (8193_{dec})	
Value	Ones, GP_ONES
Access	Read
Description	Constant with ones • –1 if this is declared as "signed int" • MAXVALUE if it is declared as "unsigned int"

Table 168: Register address 0x2002

Register address 0x2002 (8194_{dec})	
Value	1,2,3,4, GP_1234
Access	Read
Description	This constant value is used to test the Intel/Motorola format specifier. If the master reads a value of 0x1234, then with Intel format is selected – this is the correct format. If 0x3412 appears, Motorola format is selected.

Table 169: Register address 0x2003

Register address 0x2003 (8195_{dec})	
Value	Mask 1, GP_AAAA
Access	Read
Description	This constant is used to verify that all bits are accessible to the fieldbus master. This will be used together with register 0x2004.

Table 170: Register address 0x2004

Register address 0x2004 (8196_{dec})	
Value	Mask 1, GP_5555
Access	Read
Description	This constant is used to verify that all bits are accessible to the fieldbus master. This will be used together with register 0x2003.

Table 171: Register address 0x2005

Register address 0x2005 (8197_{dec})	
Value	Maximum positive number, GP_MAX_POS
Access	Read
Description	Constant in order to control arithmetic.

Table 172: Register address 0x2006

Register address 0x2006 (8198_{dec})	
Value	Maximum negative number, GP_MAX_NEG
Access	Read
Description	Constant in order to control arithmetic

Table 173: Register address 0x2007

Register address 0x2007 (8199_{dec})	
Value	Maximum half positive number, GP_HALF_POS
Access	Read
Description	Constant in order to control arithmetic

Table 174: Register address 0x2008

Register address 0x2008 (8200_{dec})	
Value	Maximum half negative number, GP_HALF_NEG
Access	Read
Description	Constant in order to control arithmetic

Table 175: Register address 0x3000 to 0x5FFF

Register address 0x3000 to 0x5FFF (12288_{dec} to 24575_{dec})	
Value	Retain range
Access	Read/write
Description	These registers can be accessed as the flag/retain range